REMARKS

Reconsideration and allowance of the above-identified application, as currently amended, is respectfully requested.

By the above-made amendments claims 1-7, 9-14 and 22-24 are now pending, of which claims 1, 3, 4 and 9-11 were amended and claims 30-32 were newly presented. Regarding independent claims 1 and 9, the subject matter of the corresponding dependent claims 8 and 15 were incorporated therein, respectively, but, however, in a manner more clearly defining of the invention intended to be covered. Correspondingly, dependent claims 8 and 15 were cancelled. The remaining changes to the claims are, basically, of a minor editorial formatting nature as well as to correct an informality therein. For example, in independent claim 3, punctuations were effected therein and, also, the expression "the impurity..." was appropriately revised to the expression an impurity.... In independent claim 4, "10", which was inadvertently added in the earlier submitted Preliminary Amendment, was appropriately deleted from this claim. Punctuations were also implemented in dependent claim 10. With regard to dependent claim 11, the expression "opposite to said first conductivity type" was deleted therefrom noting that the expression "second conductivity type" was previously defined as being "opposite to said first conductivity type", in intervening claim 10. Dependent claim 30, 31 and 32, which were newly added, are based on the limiting aspects set forth in dependent claim 12 but, however, are combined differently therefrom.

According to the outstanding Office Action, claims 1, 2, 5-11 and 13-21 stand rejected under 35 U.S.C. 102(b), allegedly, as anticipated by Kaya, et al. (U.S. Patent No. 5,821,581); claims 1 and 3 stand rejected under 35 U.S.C. 102(e),

allegedly, as anticipated by Mihnea, et al. (U.S. Patent No. 6,449,189 B2); and claims 4 and 12 stand rejected under 35 U.S.C. 103(a), allegedly, as unpatentable over the combination of Kaya, et al. (supra) in view of Ogura, et al. (U.S. Patent 6,388,293 B1). As will be shown below, the invention according to claims 1-7, 9-14 and 30-32 could not have been anticipated or rendered obvious such as alleged in the outstanding rejections. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

In accordance with independent claims 1 and 9, the invention calls for (1) the non-volatile semiconductor memory to be enabled to realize a charge holding operation in which the charges are held in the "second insulator"; (2) in the writing operation electrons are injected into the second insulator; and (3) in the erasing operation holes are injected into the second insulator. Such featured aspects which were contained in previously pending claims 8 and 15 have been appropriately re-presented in the corresponding base claims 1 and 9, thereof, respectively. It is submitted, a schemed non-volatile semiconductor memory device construction according to independent claims 1 and 9 which set forth, among the featured aspects thereof, structural characteristics in which a writing operation as well as an erasing operation require the injection of charges into the second insulator (e.g. ONO insulator 15 of the memory MISFET in Figs. 13, 16, etc.) and which further call for the charge holding function to be associated with the second insulator, was neither disclosed or suggested by Kaya, et al. or, for that matter, even over the combined teachings of Kaya, et al. and the other above-named citations. It is submitted, also, that the dependent claims are patentable for the same and similar

reasons.

Comparing the featured aspects as presently called for in claims 1+ and 9+ and that featured by Kaya, et al. clearly evidences the differences between them. For example, in the present invention, the charges are held in the "second insulator" (e.g., 61-62 held in laminated insulator 15 in Fig. 21), whereas according to Kaya, et al. the charges are held in the floating gate. As stated by Kaya, et al. "during the write process hot electrons are injected into floating gate 18...." (Column 4, lines 37-39, in Kaya, et al.) Secondly, in accordance with present invention the erasing operation is effected in a manner in which "holes are injected into the second insulator (e.g. gate insulator 15). On the other hand, according Kaya, et al's. scheme, in an erase operation, electrons are discharged from the floating gate to the source region by tunneling action through the insulator, in clear contradistinction with that set forth in each of independent claims 1 and 9 and further according to the corresponding dependent claims thereof, respectively. (Column 4, lines 55-59, in Kaya, et al.)

With regard to a point of clarification of the invention, as currently set forth, the revised "wherein" clauses in claims 1 and 9 represent structurally defining characteristics associated with the set forth non-volatile semiconductor memory. That is, these clauses represent structurally characterizing aspects of the invention claimed and do not merely involve the intended use. An example discussion regarding the featured aspects discussed above can be seen with regard to related discussion pertaining to Figs. 16+ as it relates to the first disclosed embodiment of the invention, although not limited thereto.

Kaya, et al. discloses a non-volatile memory scheme in which, as explained

above, electrons are held in the floating gate such as floating gate 18 in Fig. 1 thereof, which is a conductive film layer and not an insulator such as the gate insulator 15 shown in Figs. 13, 16, 17, etc., of the present application, which relates to the set forth "second insulator" of the present invention.

In comparison with electrons, it has been known that holes can lead to substantial damage to an oxide film when the holes pass through the oxide film. When an oxide film is damaged in this way, the insulation characteristic associated therewith becomes weakened to the point where leakage paths occur between the electron-accumulating film and the substrate. When holes occur in a scheme according to Kaya, et al., i.e., a non-volatile memory construction in which electrons are held in the floating gate (a conductive film), the held electrons flow into the substrate from the floating gate through the leakage path of the intervening oxide film, which would lead to loss of information (data) associated with that non-volatile memory cell. In accordance with the present invention however, it is the insulator or "second insulator", not the conductor, that has the charge holding function. That is, the electrons such as in connection with the writing operation are held therein and, thereby, cannot move freely. Therefore, even if a leakage path has resulted in the oxide film, the electrons can still be held within the insulator, which enhances the integrity of the storage state of the non-volatile memory cell. The write state is erasable by the holes injected in the insulator or "second insulator." Such a scheme as that now set forth in claims 1+ and 9+ was neither disclosed nor suggested by Kaya, et al.

It is submitted, also, the invention could not have been realized even if the teachings of Kaya, et al. would have been applied in combination with Mihnea, et al.

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and Ogura, et al. As to the rejection of claims 1 and 3 over Mihnea, et al., alone, as well as the rejection of claims 4 and 12 over the combined teachings of Kaya, et al. and Ogura, et al. they have been rendered moot in view of the amendments made to the base claims 1 and 9, as discussed above. In this regard it is noted that Ogura, et al. was cited, allegedly, as disclosing "a three-layer ONO layer". A three-layer structure is discussed in column 7, lines 33-36, in Ogura, et al. It is submitted, however, Ogura, et al. does not overcome the deficiencies in Kaya, et al., such as discussed above. Likewise, Mihnea, et al. is also inapplicable for the same and similar reasons therefor. For example, it is alleged that the "second insulator" according to the present invention, among the set forth featured aspects thereof, is met by insulator 151 in Mihnea, et al., which insulator is interposed between the floating gate electrode 148 and the control gate 154. However, the set forth "first gate" and "second gate" according to the present invention are formed above the "first channel region via a first insulator" and the "second channel region via a second insulator," respectively, which is clearly unlike that according to Mihnea, et al. For at least the above reasons, the invention could not have been anticipated and, moreover, could not have been realized in the manner as that alleged in the outstanding rejections.

Regarding the previously standing rejections directed to claims 8, 15 and 16-21, they have been rendered moot in view of the canceling of these claims. It should be noted, however, agreeing to the canceling of these claims should not be construed as acquiescence with regard to the merits of the rejections thereto.

Therefore, in view of the amendments presented hereinabove, reconsideration and withdrawal of the outstanding rejections as well as favorable

action on the currently pending claims together with an early formal notification of allowability of the above-identified application is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (843.43311X00).

Respectfully submitted,
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